Application No.: 10/643,164 Docket No.: 102323-0130

AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1 to 46 (Canceled)

47. (Currently Amended) A system for performing a fast Fourier transform on N ordered inputs in n stages comprising:

a non-final stage calculating means for repetitively performing in-place butterfly calculations for n-1 stages;

a final stage calculating means for performing a final stage of butterfly calculations including:

a first loop means for performing a portion of the final stage butterfly calculations, the first loop means performing [[the]] a set of butterfly calculations, and storing butterfly calculation outputs in shuffled order in place of the selected inputs to result in a correct ordering of transform outputs; and

a second loop means for performing a remaining portion of the final stage butterfly calculations, the second loop means performing two sets of butterfly calculations, and storing butterfly calculation outputs from a first one of the two sets of butterfly calculations in shuffled order in place of the inputs selected for a second one of the two sets of butterfly calculations and storing butterfly calculation outputs from the second one of the two sets of butterfly calculations in shuffled order in place of the inputs selected for the first one of the two sets of butterfly calculations to result in a correct ordering of transform outputs.

48. (Previously Presented) The system of claim 47, wherein the final stage calculating means performs all butterfly calculations as radix-4 butterflies having four inputs and four outputs.

49. (Previously Presented) The system of claim 48, wherein N is a power of two.

50. (Currently Amended) A system for performing a fast Fourier transform on N ordered inputs in n stages comprising:

a non-final stage calculating means for repetitively performing in-place butterfly calculations for n-1 stages;

a final stage calculating means for performing a final stage of butterfly calculations including:

a first loop means for performing a portion of the final stage butterfly calculations, the first loop means performing [[the]] a set of butterfly calculations, and storing butterfly calculation outputs in shuffled order in place of the selected inputs to result in a correct ordering of transform outputs; and

a second loop means for performing a remaining portion of the final stage butterfly calculations, the second loop means performing two sets of butterfly calculations, and storing butterfly calculation outputs from a first one of the two sets of butterfly calculations in shuffled order in place of the inputs selected for a second one of the two sets of butterfly calculations and storing butterfly calculation outputs from the second one of the two sets of butterfly calculations in shuffled order in place of the inputs selected for the first one of the two sets of butterfly calculations to result in a correct ordering of transform outputs,

wherein N is a power of two, and

[The system of claim 49,] wherein the non-final stage calculating means performs a first stage of radix-8 butterfly calculations followed by n-2 stages of radix-4 butterfly calculations.

51. (Currently Amended) The system of claim 48, wherein the non-final and final stage calculating means include a four-fold single instruction multiple data (SIMD) processor

for performing four radix-4 butterfly calculations at a time.

Claims 52 – 57 (Cancelled)